WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a gate wiring formed over an insulating surface;

an insulating film formed over the gate wiring;

a first amorphous semiconductor film formed over the insulating film;

a source region and a drain region provided in a second amorphous semiconductor film containing an impurity element of one conductivity type, formed over the first amorphous semiconductor film;

one of a source wiring and an electrode, provided on one of the source region and the drain region; and

a pixel electrode formed so as to partially overlap and be in contact with the electrode,

wherein an end of the first amorphous semiconductor film has a tapered shape.

2. A semiconductor device comprising:

a gate wiring formed over an insulating surface;

an insulating film formed over the gate wiring;

a first amorphous semiconductor film provided over the insulating film;

a source region and a drain region provided in a second amorphous semiconductor film containing an impurity element of one conductivity type, provided over the first amorphous semiconductor film;

one of a source wiring and an electrode, provided over one of the source region and the drain region; and

a pixel electrode provided so as to partially overlap and be in contact with the electrode,

wherein one of an end of the first amorphous semiconductor film and an end of the second amorphous semiconductor film has a tapered shape.

3. A semiconductor device according to claim 1 or claim 2 wherein the side edge of the first amorphous semiconductor film having a tapered shape has an angle in the range of 5° to 45°.

4. A semiconductor device comprising:

a gate wiring formed over an insulating surface;

a gate insulating film formed over the gate wiring;

an amorphous semiconductor film formed over the gate insulating film;

a source region and a drain region, formed over the amorphous semiconductor film;

one of a source wiring and an electrode, formed over one of the source region and the drain region; and

a pixel electrode formed so as to partially overlap and be in contact with the electrode,

wherein a region overlapping with the gate wiring with the gate insulating film therebetween and not overlapping with the source region or the drain region in the amorphous semiconductor film is thinner than other region and is tapered to become thinner toward a center of the region.

5. A semiconductor device according to claim 4 wherein the region tapered has an

angle in the range of 5° to 45°.

6. A semiconductor device according to claim 4 or claim 5 wherein the side edge of the first amorphous semiconductor film has a taper shape with an angle in the range of 5° to 45°.

7. A semiconductor device according to claims 1 to 6 wherein a side face of one of the source region and the drain region is aligned with one of the source wiring and the electrode.

8. A method of manufacturing a semiconductor device, comprising:

a first step of forming a gate wiring over an insulating surface;

a second step of forming an insulating film covering the insulating surface and the gate wiring;

a third step of forming a first amorphous semiconductor film over the insulating film;

a fourth step of forming a second amorphous semiconductor film containing an impurity element of one conductivity type over the first amorphous semiconductor film;

a fifth step of forming a conductive film comprising metallic material over the second amorphous semiconductor film; and

a sixth step of etching the conductive film and the first amorphous semiconductor film and the second amorphous semiconductor film to form a side edge of the first amorphous semiconductor film into a taper shape;

a seventh step of forming a transparent conductive film over the conductive film; and

an eighth step of etching a part of the first amorphous semiconductor film and the transparent conductive film and the conductive film and the second amorphous semiconductor film to expose a part of the first amorphous semiconductor film and to form a pixel electrode from the transparent conductive film and form a source wiring from the conductive film and form source region and drain region from the second amorphous semiconductor film.

9. A method of manufacturing a semiconductor device, comprising:

a first step of forming a gate wiring over an insulating surface;

a second step of forming an insulating film covering the insulating surface and the gate wiring;

a third step of forming a first amorphous semiconductor film over the insulating film;

a fourth step of forming a second amorphous semiconductor film containing an impurity element of one conductivity type over the first amorphous semiconductor film;

a fifth step of forming a conductive film comprising metallic material over the second amorphous semiconductor film;

a sixth step of etching the insulating film and the first amorphous semiconductor film and the second amorphous semiconductor film and the conductive film to form a side edge of the first amorphous semiconductor film into a taper shape;

a seventh step of forming a transparent conductive film over the conductive film; and

an eighth step of etching a part of the first amorphous semiconductor film and the transparent conductive film and the conductive film and the second amorphous semiconductor film to expose a part of the first amorphous semiconductor film and to form a pixel electrode

from the transparent conductive film and form a source wiring from the conductive film and form a source region and a drain region from the second amorphous semiconductor film.

10. A method of manufacturing a semiconductor device according to claim 8 or claim 9 wherein in the sixth step, the conductive film and the second amorphous semiconductor film and the first amorphous semiconductor film are etched with a chlorine type gas.

11. A method of manufacturing a semiconductor device according to any one of claims 8 to 10 wherein in the eighth step, a part of the first amorphous semiconductor film and the conductive film and the second amorphous semiconductor film are etched with a chlorine type gas.

12. A method of manufacturing a semiconductor device according to any one of claims 8 to 11 wherein the chlorine type gas is selected from Cl_2 and BCl_3, HCl and $SiCl_4$ or a gas containing a plurality of gases selected from these gases.

13. A method of manufacturing a semiconductor device, comprising:

a step of forming a gate wiring over an insulating surface;

a step of forming an insulating film over the insulating surface and the gate wiring;

a step of forming a first amorphous semiconductor film over the insulating film;

a step of forming a second amorphous semiconductor film containing an impurity element of one conductivity type over the first amorphous semiconductor film;

a step of forming a conductive film over the second amorphous

semiconductor film; and

a step of etching the conductive film and the first amorphous semiconductor film and the second amorphous semiconductor film to form a side edge of the first amorphous semiconductor film into a taper shape;

a step of forming a transparent conductive film over the second amorphous semiconductor film; and

a step of etching the transparent conductive film and the conductive film and the second amorphous semiconductor film to form a source wiring and a source region and a drain region,

wherein the conductive film contains aluminum or titanium, and

wherein the first amorphous semiconductor film is etched into a taper shape with a mixture gas Cl_2 and BCl_2.

14. A method of manufacturing a semiconductor device, comprising:

a step of forming a gate wiring over an insulating surface;

a step of forming an insulating film over the insulating surface and the gate wiring;

a step of forming a first amorphous semiconductor film over the insulating film;

a step of forming a second amorphous semiconductor film containing an impurity element of one conductivity type over the first amorphous semiconductor film;

a step of forming a conductive film over the second amorphous semiconductor film;

a step of etching the first amorphous semiconductor film and the second amorphous semiconductor film and the conductive film to form a side edge of the first

amorphous semiconductor film into a taper shape;

a step of forming a transparent conductive film over the second amorphous semiconductor film;

a step of etching the transparent conductive film and the conductive film and the second amorphous semiconductor film to form a source wiring and a source region and a drain region,

wherein the conductive film contains at least tantalum, and

wherein the first amorphous semiconductor film is etched into a taper shape with a mixture gas of Cl_2 and CF_4.

15. A method of manufacturing a semiconductor device, comprising:

a step of forming a gate wiring over an insulating surface;

a step of forming an insulating film over the insulating surface and the gate wiring;

a step of forming a first amorphous semiconductor film over the insulating film;

a step of forming a second amorphous semiconductor film containing an impurity element of one conductivity type over the first amorphous semiconductor film;

a step of forming a conductive film over the second amorphous semiconductor film;

a step of etching the first amorphous semiconductor film and the second amorphous semiconductor film and the conductive film to form a side edge of the first amorphous semiconductor film into a taper shape;

a step of forming a transparent conductive film over the second amorphous semiconductor film; and

a step of etching the transparent conductive film and the conductive film and the second amorphous semiconductor film by etching to form a source wiring and a source region and a drain region,

wherein the conductive film contains at least tungsten, and

wherein the first amorphous semiconductor film is etched into a taper shape with a mixture gas of Cl_2 and CF_4 and O_2 or a mixture gas of Cl_2 and SF_6 and O_2.